Amendments to the Specification

Please replace the abstract with the following amended abstract.

ABSTRACT OF THE DISLCOSURE

A method for determining the validity of microprocessor instructions is disclosed wherein numerous means can be employed to calculate the number of valid instructions contained within an instruction bundle. ~~Methods and systems are disclosed for calculating the number of valid instructions in a microprocessor instruction bundle.~~ One method advances in the instructions along the pipeline and edge detects the number of valid instructions with the pipeline. Another method fetches a bundle of instructions, shifts instructions within the bundle, and edge detects the valid instructions. Still another method fetches the bundle of instructions and detects a complex instruction within the bundle. Instructions occurring after the complex instruction are shifted, and the number of valid instructions occurring after the complex instruction are edge detected.

Please replace the title of the application with the following title:

Methods for Determining Valid Microprocessor Instructions in an Instruction Bundle.

Please replace paragraph [0001] with the following amended paragraph

[0001] This invention generally relates to computer systems and, more particularly, to methods ~~and to systems~~ for calculating the number of valid instructions within a microprocessor instruction bundle.

Please replace paragraph [0013] with the following amended paragraph:

[0013] Those of ordinary skill in the art also understand the present invention is not limited to any particular manufacturer's microprocessor design. Sun Microsystems, for example, designs and manufactures high-end 64-bit and 32-bit microprocessors for networking and intensive computer needs (Sun Microsystems, Inc., 901 San Antonio Road, Palo Alto CA 94303~~,~~

~~www.sun.com~~). Advanced Micro Devices (Advanced Micro Devices, Inc., One AMD Place, P.O. Box 3453, Sunnyvale, California 94088-3453, 408.732.2400, 800.538.8450, ~~www.amd.com~~) and Intel (Intel Corporation, 2200 Mission College Blvd., Santa Clara, California 95052-8119, 408.765.8080, ~~www.intel.com~~) also manufacture various families of microprocessors. Other manufacturers include Motorola, Inc. (1303 East Algonquin Road, P.O. Box A3309 Schaumburg, IL 60196, ~~www.Motorola.com~~), International Business Machines Corp. (New Orchard Road, Armonk, NY 10504, (914) 499-1900, ~~www.ibm.com~~), and Transmeta Corp. (3940 Freedom Circle, Santa Clara, CA 95054, ~~www.transmeta.com~~). While only one microprocessor is shown, those skilled in the art also recognize the present invention is applicable to computer systems utilizing multiple processors.

Please replace paragraph [0021] with the following amended paragraph:

[0021] FIG. 6 is a block diagram illustrating one embodiment of the present invention for determining the number of valid instructions 86 within the instruction bundle 84. When the complex instruction 88 is detected, the original instruction bundle 84 is broken at the instruction prior to the complex instruction 88. FIG. 6A shows, therefore, the original instruction bundle 84 is broken at instruction #2. Instructions #1 and #2 are treated as a first new instruction bundle 92, shown in FIG. 6B, with all other instructions in the first new instruction bundle 92 marked as invalid instructions 90. Because the first new instruction bundle 92 is monotonic — that is, all the valid instructions, and corresponding valid bits, are compressed at the "top" of the bundle 92 — the number of valid instructions in the bundle 92 may be edge detected. An edge detection circuit 91 may be used to detect when the string of valid bits, corresponding to each valid instructions, transitions from high ("1") to low ("0"). The monotonic nature of the bundle ensures any valid instructions will lie from the first instructions slot #1 and onward. Once an invalid instruction is encountered, every instruction afterwards will be invalid. The edge detect circuit 91 , therefore, detects a "1" to "0" transition and stops — there's no need to population count the number of valid bits in each slot in the bundle. During a first clock cycle, therefore, the valid instructions #1 and #2, of the first new instruction bundle 92, are sent for execution along the pipeline.